wherein, when the device is powered, each of the plurality of first circuits is in the standby state, and

wherein the one of the first circuits is enabled to be accessed by the second circuit when the power control circuit issues an acknowledgement to the second circuit according to the request.

18. The semiconductor integrated circuit device according to claim 17, wherein, when the power control circuit issues the acknowledgement to the second circuit, the power control circuit issues a power control signal to the one of the first circuits so that the one of the first circuits is enabled to operate.

19. The semiconductor integrated circuit device according to claim 17, wherein when the power control circuit issues the acknowledgement where a preset maximum power is satisfied.

20. The semiconductor integrated circuit device according to claim 17, wherein, when the first circuit is in the standby state, no clock is supplied to the first circuit.

21. The semiconductor integrated circuit device according to claim 17, wherein, when the first circuit is in the standby state, no supply voltage is supplied to the first circuit.

22. The semiconductor integrated circuit device according to claim 17, wherein, when the first circuit is in the standby state, leakage current is suppressed.

23. A power control method of a semiconductor integrated circuit device, comprising:

providing the semiconductor integrated circuit device including a power control circuit, a plurality of first circuits, each of the plurality of first circuits having at least an active state and a standby state, and a second circuit to be privileged to access each of the first circuits

setting each of the plurality of first circuits in the standby state when the device is powered,

issuing a request to the power control circuit by the second circuit in order to access one of the first circuits; and

issuing an acknowledgement to the second circuit by the power control circuit so that the one of the first circuits is enabled to be accessed by the second circuit.

24. The power control method according to claim 23, wherein, when the power control circuit issues the acknowledgement to the second circuit, the power control circuit issues a power control signal to the one of the first circuits so that the one of the first circuits is enabled to operate.

25. The power control method according to claim 23, wherein when the power control circuit issues the acknowledgement where a preset maximum power is satisfied.

26. The power control method according to claim 23, wherein, when the first circuit is in the standby state, no clock is supplied to the first circuit.

27. The power control method according to claim 23, wherein, when the first circuit is in the standby state, no supply voltage is supplied to the first circuit.

28. The power control method according to claim 23, wherein, when the first circuit is in the standby state, leakage current is suppressed.